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06ES32

Third Semester B.E. Degree Examination, December 2010
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO Questions from each of Part – A and Part - B.***

PART - A

1 a. What is an equivalent circuit of a device? Explain the different equivalent circuits for semiconductor diode. **(07 Marks)**

b. Analyse the circuit shown below, Fig. Q1(b), and draw the output waveform. Assume $V_r = 0.7V$. **(08 Marks)**

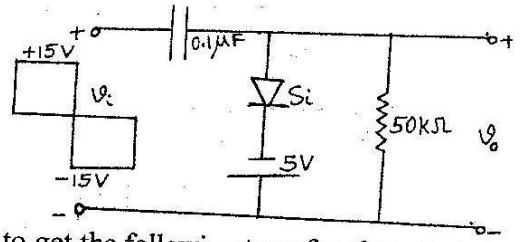

Fig. Q1(b)

c. Write a suitable circuit to get the following transfer characteristics fig. Q1(c), and explain its working. **(05 Marks)**

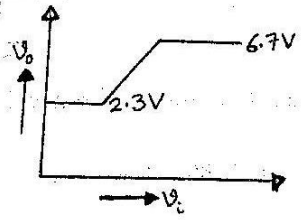

Fig. Q1(c)

2 a. Find I_{C_Q} and V_{CE_Q} for the circuit shown, Fig. Q2(a). **(05 Marks)**

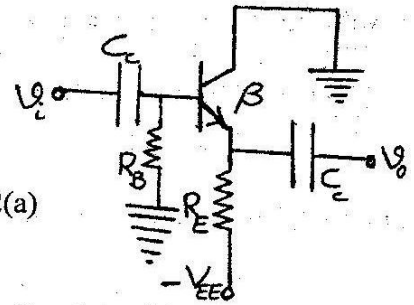

Fig. Q2(a)

b. Find the coordinates of the Q point and locate it on the dc load line for the voltage divider configuration. Given $V_{CC} = 16V$, R_1 (upper resistor) = 62 kΩ , $R_2 = 9.1$ kΩ , $R_C = 3.9$kΩ , $R_E = 0.68$kΩ and $\beta = 80$. The coupling capacitors are 10μF each. Also find V_C , V_E and V_B. **(08 Marks)**

c. Define turn ON time and turn OFF time of a transistor. Design a transistor inverter if $V_{CC} = 10V$, $I_{C_{sat}} = 10mA$ and $\beta = 250$. Assume input to be a pulse of amplitude 10V. **(07 Marks)**

3 a. What is bias stabilization? Explain. Derive an expression for $S(I_{CO})$ and $S(V_{BE})$ for fixed bias configuration. **(08 Marks)**

b. For an emitter bias circuit (capacitor is bypassed), determine r_e, Z_i, Z_o and A_v. Given $R_B = 470\ k\Omega$, $R_C = 2.2k\Omega$, $V_{CC} = 20V$, $R_E = 0.56k\Omega$, $C_E = 10\mu F$, $\beta = 120$, $r_o = 40k\Omega$, $C_C = 10\mu F$. **(08 Marks)**

c. Determine i) the common logarithm of the number 2.2×10^3. ii) the power gain in decibels for $P_o = 100$ m watts , $P_i = 5$m watts. **(04 Marks)**

4 a. The transistor is connected as a CE amplifier. Determine Z_c, Z_o, A_I and A_V using complete hybrid model. **(10 Marks)**

b. Discuss the low frequency and high frequency response of a RC coupled amplifier. **(10 Marks)**

PART - B

5 a. For the circuit of fig. Q5(a), calculate the dc bias voltage V_E. **(05 Marks)**

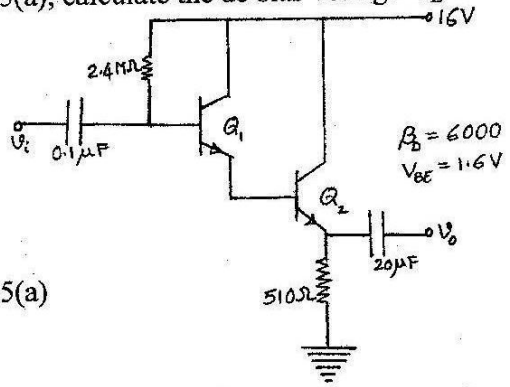

Fig. Q5(a)

b. With a block diagram, explain the difference between voltage series and voltage shunt feedback. **(05 Marks)**

c. Using the block diagram approach, derive an expression for A_f and Z_{of} for current series feedback amplifier. **(10 Marks)**

6 a. With a neat circuit diagram, explain the operation of a transformer coupled class A power amplifier. **(10 Marks)**

b. For a class B amplifier with $V_{CC} = 25V$ driving an 8Ω load, determine i) maximum I/P power ii) maximum O/P power iii) maximum circuit efficiency. **(06 Marks)**

c. Calculate the second harmonic distortion for an O/P waveform having measured values of $V_{CE_{min}} = 2.4V$, $V_{CE_Q} = 10V$ and $V_{CE_{max}} = 20V$. **(04 Marks)**

7 a. With a neat circuit diagram, explain the working principle of RC phase shift oscillator, with relevant equations. **(10 Marks)**

b. What are the tuned oscillators? Explain any one type of tuned oscillator. **(10 Marks)**

8 a. Define g_m and r_d of field effect transistor. Explain the procedure to determine the above values graphically. **(06 Marks)**

b. Write the ac equivalent circuit for voltage divider JFET configuration and determine Z_i, Z_o and A_v. **(10 Marks)**

c. Differentiate between enhancement and depletion MOSFET. **(04 Marks)**

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